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Application of:	Craig E. Hampel	Confirmation No.:	8955
Serial No.:	10/676,648	Art Unit:	3691
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For:	Integrated Circuit with Bi-Modal Data Strobe	Attorney Docket No.:	60809-0099-US
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PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is being filed prior to the receipt of any Office Action for the above identified patent application.

The Commissioner has been authorized through the electronic filing system to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0310 (order no. 60809-0099-US).

IN THE SPECIFICATION

Revise paragraph 0051 as follows:

As indicated above, when the DRAM 440 is configured to use the DS leads 170 in a unidirectional manner, the data output by the DRAM 440 is clocked by the data strobe generated by a controller (e.g., controller 110). This is possible because the data strobe is always transmitted by the controller. Additionally, the data strobe typically suffers from less phase shift than the clock, and as a result the rate of data transmission over the memory bus may be increased over that of prior systems. In this mode, the DRAM 440 is compatible with controllers (such as the controllers described herein) configured to continuously transmit a data strobe to the DRAM 440. But when the DRAM 440 is configured to use the DS leads 170 in a ~~unidirectional~~ bidirectional manner, the data strobe is not available while the DRAM 440 transmits data. Instead, the data output by the DRAM 440 is clocked by the clock. In this mode, the DRAM 440 is compatible with conventional controllers (e.g., controller 110).

Revise paragraph 0044 as follows:

The DRAM mode register 302 stores a directional mode when used in conjunction with the DRAM 130 (or the DRAM 440 of FIG. 4). The directional mode determines whether the DS leads 170 are unidirectional or bidirectional. The mode register 302 may preferably be set during operation of the DRAM 130 by the controller 110 or during the manufacture of the DRAM 130 or memory module 120. In some embodiments, the controller 110 and DRAM 130 are configured so that the controller may send a command over the control and address lines 150 that directs the DRAM to store a particular mode value in the mode register 302. The directional mode stored by the mode register 302 is transmitted to the AND gate 305 ~~304~~.

Revise paragraph 0045 as follows:

The AND gate 305 ~~304~~, as indicated in the preceding paragraph, receives input from the DRAM mode register 302. The AND gate 305 ~~304~~ also receives input from the transmit (Tx) indicator 320. The output of the AND gate 305 ~~304~~ is high if the directional mode is high and the transmit (Tx) indicator 320 is high. Preferably, the transmit (Tx) indicator 320 and the directional mode are high when the DRAM 130 transmits a data strobe to the

controller and the DRAM 130 is configured to operate in a bidirectional mode. The output of the AND gate 305 ~~304~~ is connected to the output buffer 325 to enable or disable the output buffer 325. So when the DRAM 130 transmits data and, in addition, the DRAM 130 is configured to operate in a bidirectional mode, the output buffer 325 is enabled and drives the received clock signal onto the DS lead 170 as the data strobe for the data being transmitted from the data out register 370. Conversely, when the DRAM 130 is configured to operate in a unidirectional mode, the output of the AND gate 305 ~~304~~ is low such that the output buffer 325 is disabled. When the output buffer 325 is not enabled, its output is tristated (i.e., set to a high impedance state), which leaves the DS lead 170 floating if no other device is asserting a signal on the DS lead, and more generally allows the DS lead 170 to be driven by another device (e.g., the memory controller 110, or another memory device in another memory module on the same memory bus as the memory module 120 in which the DRAM 130 resides).

Revise paragraph 0054 as follows:

FIG. 5B illustrates another embodiment of a DRAM 450 for use in the memory system 100. Unlike the DRAMs 130, 440 of FIGS. 3 and 4, this DRAM 450 does not include an AND gate 305 ~~304~~ or an output buffer 325. This is because this DRAM 450 does not transmit a data strobe over the DS lead 170. Additionally, this DRAM 450 does not include a multiplexor 410 because the output of the data-out register 370 is not clocked or timed by the clock. Instead, the data-out register 370, like the data-in register 340, is always clocked by a data strobe transmitted over the DS lead 170. Preferably, only control and address signals transmitted over the C/A lead 150 are clocked by the clock. This DRAM 450 is compatible with controllers described herein (e.g., controller 110 and controller 425), but is not compatible with conventional controllers.